

1    WHAT IS CLAIMED IS:

1                   1.       A method of writing to a dual-port memory, the method comprising:  
2                   providing a data bit on a data line, and a complement of the data bit on a  
3   complementary data line;  
4                   selecting a word line to activate a first device coupled to the data line and a  
5   second device coupled to the complementary data line; and  
6                   selecting a column select line to activate a third device coupled between the first  
7   device and a first node of a memory cell, and a fourth device coupled between the second device  
8   and a second node of the memory cell.

1                   2.       The method of claim 1 further comprising:  
2                   before selecting the column select line, asserting a write enable.

1                   3.       The method of claim 2 further comprising:  
2                   deselecting the write enable; and  
3                   deactivating the third device and the fourth device.

1                   4.       The method of claim 3 wherein the first, second, third, and fourth devices  
2   are NMOS devices.

1                   5.       The method of claim 1 wherein the word line further couples to a read  
2   cell.

1                   6.       A method of determining the presence of a match between a data entry  
2   and a comparand in a content addressable memory, the content addressable memory comprising  
3   a plurality of memory storage cells arranged in rows and columns, each memory storage cell  
4   having a write circuit and a read circuit, wherein the write circuit and the read circuit of each  
5   memory storage cell in a row is coupled to one word line, and wherein the read cells of each  
6   memory storage cell in a column are coupled to one first read line and one second read line, the  
7   method comprising:  
8                   writing the data entry to odd numbered memory storage cells in a column of  
9   memory storage cells;

10 writing a complement of the data entry to even numbered memory storage cells in  
11 the column of memory storage cells;  
12 driving word lines coupled to the even numbered memory storage cells in the  
13 column of memory storage cells with the comparand; and  
14 driving word lines coupled to the odd numbered memory storage cells in the  
15 column of memory storage cells with a complement of the comparand.

1 7. The method of claim 5 further comprising:  
2 determining a parallel impedance of the read cells in the column of memory  
3 storage cells, and outputting a match is the impedance is high..

1 8. The method of claim 6 further comprising decoding the position of the  
2 column of the match as a binary word.

1 9. The method of claim 7 wherein the data entries are product terms.

1 10. A method of writing to a dual-port memory comprising:  
2 providing a data bit on a data line, and a complement of the data bit on a  
3 complementary data line;  
4 asserting a write enable signal, which asserts a column select line thus activating a  
5 first and second device; and  
6 asserting a word line thus activating a third and fourth device,  
7 wherein the first and third devices are coupled between the data line and a first  
8 node of a memory cell, and the second and fourth devices are coupled between the  
9 complementary data line and a second node of the memory cell.

1 11. The method of claim 10 wherein a gate of the third device and a gate of  
2 the fourth device are coupled to the word line, and the third device is coupled to the data line and  
3 the fourth device is coupled to the complementary data line.

1 12. The method of claim 11 wherein the word line further couples to a read  
2 cell.

1                   13.     The method of claim 12 wherein a gate of the first device and a gate of the  
2 second device couple to the column select line.

1                   14.     The method of claim 13 wherein the first, second, third, and fourth devices  
2 are NMOS devices.

1                   15.     A method of reading data in a dual port memory comprising:  
2 selecting a word line thus activating a first device; and  
3 sensing an impedance between a first node and a second node,  
4 wherein the first device and a second device are coupled in series between the  
5 first node and the second node, the second device having a gate coupled to a first node in a  
6 memory cell, and  
7 wherein the word line couples to a third device and a fourth device, the third  
8 device and fourth devices used for writing to the memory cell.

1                   16.     The method of claim 15 wherein the third device couples between a data  
2 line and a fifth device and the fourth device couples between a complementary data line and a  
3 sixth device.

1                   17.     The method of claim 16 wherein the fifth device couples to the first node  
2 in the memory cell and the sixth device couples to a second node in the memory cell.

1                   18.     The method of claim 17 wherein a gate of the fifth device and a gate of the  
2 sixth device are coupled to a column select line, the column select line enabled by a write enable  
3 signal.

1                   19.     The method of claim 18 wherein the memory cell comprises a first  
2 inverter having an input and an output and a second inverter having an input and an output, the  
3 input of the first inverter coupled to the output of the second inverter, and the input of the second  
4 inverter coupled to the output of the first inverter.

1                   20.     The method of claim 15 wherein the first and second devices are NMOS  
2 devices.